IGOR G. KOUZNETSOV, Ph.D.
Electrical Engineer
San Francisco, CA, 94109 • e-mail: igorgk2010@gmail.com • mobile: 415.713.3882

SUMMARY

Dr. Igor Kouznetsov is a results-oriented and business-minded expert in the field of semiconductor system-on-a-chip (SoC) and memory technology. As a member of IEEE's Electron Devices Society (EDS) and IEEE Solid State Circuits Society (SSCS), Dr. Kouznetsov has an established record of delivering mixed-signal technology platforms with embedded memory to production. With 24 years of experience in semiconductor devices: logic, nonvolatile memory (NVM), NOR flash, NAND flash, SRAM, microcontroller (MCU), power-management units, analog and mixed-signal circuits, touch screen controllers, and image sensors, Dr. Kouznetsov has obtained 37 issued U.S. patents. Dr. Kouznetsov has industry acquired experience and expertise in a wide variety of areas including silicon process technology development, integrated circuit design, yield improvement, defect and failure analysis, development program initiation and management, transfer to high-volume manufacturing, defining technology roadmaps, licensing of intellectual property. Dr. Kouznetsov also has substantial knowledge of integrated circuit reliability aspects, including electro-static discharge (ESD), latch-up, time-dependent dielectric breakdown (TDDB), charge to breakdown (QBD), negative/positive bias temperature instability (NBTI/PBTI), Vt-fluence, electromigration, radiation hardness, write disturbs, endurance, and data retention. In addition, Dr. Kouznetsov is a frequent presenter at conferences and authored numerous publications.

EXPERIENCE

Western Digital - Milpitas, CA 2019/01 – Present
Director of Research Operations

- Establish and supervise annual operating strategy for company's advanced research department
- Implemented new resource, procurement, and milestone management processes for highly technical projects in the areas of emerging NVM, machine learning, and RISC-V microprocessor architecture
- Designed an IP block in RTL for a silicon root-of-trust chip

Cypress Semiconductor - San Jose, CA 2004/04 – 2018/11
Senior Member of Technical Staff

- Led R&D development of a mixed-signal process platform with embedded NVM. Designed charge-trap NVM bit cell and array, sector select, row, and column drivers. Optimized charge-storing dielectric properties for fast programming speed, robust endurance, and data retention. Optimized device implants, critical dimensions, mask Boolean operations, and optical proximity correction (OPC) methods. On this platform, the company produced and shipped more than two billion SoC units over 15 years
- Assisted the CEO, CTO, and Executive VP in establishing a platform technology roadmap, contract negotiation, demand forecast, market and competitor analysis procedures and analysis metrics

- Developed go-to-market strategies for process and design IP products, created new product introduction (NPI) presentations and other marketing collateral; promoted the IP products at trade shows in US, China, and Japan
- Led product definition using customer needs, market research, competitive and trade-off analyses. Launched product and process development projects. Managed multi-functional product development team composed of design, product, test, R&D, and manufacturing engineers
- Delivered embedded NVM technology at four technology nodes from launch to successful product qualification and production ramp-up with high manufacturing yield. Multi-functional teams consisted of process, device, design, test, and product engineers. Invented circuit methods to reduce program disturbs and increase read current window in NVM
- Led multiple IP test chip and SoC product tapeouts; served as a foundry technology interface; resolved yield failures by analyzing data bit maps, schmoo plots, analog parameters, data read access time, etc.
- In a team with business unit management and legal department, negotiated and finalized four flash memory intellectual property (IP) licensing agreements with leading semiconductor foundries and fabless companies, by providing technology IP customer value calculations and live demos

Barcelona Design - Newark, CA 2002/06 – 2004/04
Senior Design Engineer

- Member of team inventing, design, and characterization of current-controlled differential ring oscillators with multi-path delay stages for compact well-matched layout and ease of porting to new CMOS technology nodes
- Supported engineering design development of phase lock loop (PLL) and analog-to-digital converter (ADC) design automation software through analysis and design model generation

Matrix Semiconductor, SanDisk - Santa Clara, CA 2001/02 – 2002/05
Member of Technical Staff

- Participated in the development of the world's first three-dimensional (3-D) nonvolatile semiconductor memory based on diode-antifuse cross-point array
- Optimized quality and thickness of the antifuse dielectric by matching its leakage to the reverse leakage of the cell selector device in the form of a polysilicon diode

Cypress Semiconductor - San Jose, CA 1998/01 – 2001/02
Senior Technology Development Engineer

- Developed standard logic and high voltage devices for charge-trap embedded flash memory technology
- Led process integration efforts during the development of a static random-access memory (SRAM) technology with shallow trench isolation (STI) and compact single word line cell architecture

EDUCATION

University of California at Berkeley
Ph.D.: Electrical Engineering and Computer Sciences, 1997/12

Dartmouth College
M.S.: Engineering Science, 1994/06
Awards: Dartmouth College Fellowship, NASA Fellowship

Moscow Institute of Physics and Technology
Diploma: Applied Mathematics and Physics, 1992/08

AREAS OF EXPERTISE

Analog Design, ASIC, BSIM3, BSIM4, C, CAD, Cadence Composer and Virtuoso, Calibre, Chisel, Clarity, Competitive Analysis, Cross Functional Leadership, Design Verification, Device Engineering, Device Modeling, DRC, EDA, Failure Analysis, FDK, Financial Analysis, FIT Rate, Flash Memory, Foundry, Integrated Circuits, Linear Algebra, LVS, Mixed Signal, Monte-Carlo Simulations, Neural Networks, Nonvolatile Memory, NPI, Numerical Methods, NVM, PLL, PDK, Process Integration, Product Development, Product Qualification, Program Management, Project Management, Radiation Hardness, Reliability Modeling, RF Design, RTL Design, SAS JMP, Semiconductors, Semiconductor Reliability, Sensors, Silicon, SPICE, SRAM, Statistical Analysis, SystemVerilog, TCAD Modeling

PROFESSIONAL AFFILIATIONS

Institute of Electrical and Electronics Engineers (IEEE)

IEEE Electron Devices Society (EDS)

IEEE Solid State Circuits Society (SSCS)

PUBLICATIONS

"Total Ionizing Dose Hardness of an 8Mbit 40nm CMOS Technology Based SONOS NOR Flash," H. Puchner, V. Prabhakar, **I. Kouznetsov**, T. Phan, V. Agrawal, K. Donnelly, and J. Tausch, submitted to IEEE Trans. Nucl. Sci.

"40 nm Ultralow-Power Charge-Trap Embedded NVM Technology for IoT Applications," **I. Kouznetsov**, K. Ramkumar, V. Prabhakar, L. Hinh, H. M. Shih, S. Saha, S. Govindaswamy, M. Amundson, D. Dalton, T. Phan, Z. Luzada, V. Raghavan, V. Agrawal, K. Donnelly, P. C. Shih, C. C. Huang, K. L. Lee, C. H. Wang, C. H. Huang, C. H. Lin, and Y. K. Sheu, in Proc. IEEE IMW, May 2018, pp. 1-4.

"Impact of Total Ionizing Dose on the Data Retention of a 65 nm SONOS-based NOR Flash," H. Puchner, P. Ruths, V. Prabhakar, **I. Kouznetsov**, S. Geha, in IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 3005-3009, Dec. 2014.

"A Scalable, Low Voltage, Low Cost SONOS Memory Technology for Embedded NVM Applications," K. Ramkumar, **I. Kouznetsov**, V. Prabhakar, K. Shakeri, X. Yu, Y. Yang, L. Hinh, S. Lee, S. Samantha, H. M. Shih, S. Geha, P. C. Shih, C. C. Huang, H. C. Lee, S. H. Wu, J. H. Gau, and Y. K. Sheu, in Proc. IEEE IMW, May 2013, pp. 199-202.

"Differential Ring Oscillators with Multipath Delay Stages," S. S. Mohan, W. S. Chan, D. M. Colleran, S. F. Greenwood, J. E. Gamble, and **I. G. Kouznetsov**, in Proc. IEEE CICC, 2005, pp. 503-506.

"Electronegativity of Low-Pressure High-Density Oxygen Discharges," J. T. Gudmundsson, **I. G. Kouznetsov**, K. K. Patel, and M. A. Lieberman," Journal of Physics D: Applied Physics, vol. 34, no. 7, p. 1100, 2001.

"Transitions and Scaling Laws for Electronegative Discharge Models," A. J. Lichtenberg, M. A. Lieberman, **I. G. Kouznetsov**, and T. H. Chung, in Plasma Sources Science and Technology, vol. 9, no. 1, p. 45, 2000.

"Internal Sheaths in Electronegative Discharges," **I. G. Kouznetsov**, A. J. Lichtenberg, and M. A. Lieberman, in Journal of Applied Physics 86, p. 4142, 1999.

"Modeling Plasma Discharges at High Electronegativity," A. J. Lichtenberg, **I. G. Kouznetsov**, Y. T. Lee, M. A. Lieberman, I. D. Kaganovich, and L. D. Tsendin, in Plasma Sources Science and Technology, vol. 6, no. 3, p. 437, 1997.

"Modelling Electronegative Discharges at Low Pressure," **I. G. Kouznetsov**, A. J. Lichtenberg, and M. A. Lieberman, in Plasma Sources Science and Technology, vol. 5, no. 4, p. 662, 1996.

"Modeling Electronegative Discharges at Low Pressure," A. J. Lichtenberg, C. Lee, M. A. Lieberman, and **I. Kouznetsov**, in Proc. IEEE International Conference on Plasma Science, 1995, p. 149.

"Radial Energy Transport by Magnetospheric ULF Waves: Effects of Magnetic Curvature and Plasma Pressure," **I. Kouznetsov** and W. Lotko, in Journal of Geophysical Research, vol. 100, issue A5, 1995.

PRESENTATIONS

"Embedded Flash for Consumer and Industrial Applications in the Age of IoT" (Tutorial, Invited), IEEE International Memory Workshop (IMW), Kyoto, Japan, May 2018.

"40 nm Ultralow-Power Charge-Trap Embedded NVM Technology for IoT Applications", IEEE International Memory Workshop (IMW), Kyoto, Japan, May 2018.

"Embedded Charge-Trap Nonvolatile Memory Technologies at 40 nm Node and beyond" (Invited), Leading-Edge Embedded NVM Workshop, Gardanne, France, September 2017.

"Embedded 28 nm Charge-Trap NVM Technology", Flash Memory Summit, Session 304-A, Santa Clara, CA, August 2017.

"Advances in Charge-Trap Nonvolatile Memory Technology" (Invited), Leading-Edge Embedded NVM Workshop, Gardanne, France, September 2015.

"Scalable, Low Voltage, Low Cost Technologies for Embedded NVM Applications", Leading-Edge Embedded NVM Workshop, Gardanne, France, September 2013.

U.S. PATENTS

10,644,021	Dense arrays and charge storage devices; Thomas H. Lee, **Igor G. Kouznetsov**
10,373,688	High voltage architecture for non-volatile memory; Georgescu Bogdan I., Moscaluk Gary P., Raghavan Vijay, **Kouznetsov Igor G.**
10,103,244	Drain extended MOS transistors with split channel; Prabhakar Venkatraman, **Kouznetsov Igor**
10,062,573	Embedded SONOS with triple gate oxide and manufacturing method of the same; Ramkumar Krishnaswamy, **Kouznetsov Igor**, Prabhakar Venkatraman, Keshavarzi Ali
10,032,517	Memory architecture having two independently controlled voltage pumps; Hirose Ryan Tasuo, Jenne Fredrick B., Raghavan Vijay, **Kouznetsov Igor G.**, Ruth Paul Fredrick, Zonte Cristinel, Georgescu Bogdan L., Gitlan Leonard Vasile, Myers James Paul
10,002,878	Complementary SONOS integration into CMOS flow; Prabhakar Venkatraman, Ramkumar Krishnaswamy, **Kouznetsov Igor**
9,997,528	Complementary SONOS integration into CMOS flow; Prabhakar Venkatraman, Ramkumar Krishnaswamy, **Kouznetsov Igor**
9,922,988	Embedded SONOS based memory cells; Ramkumar Krishnaswamy, **Kouznetsov Igor G.**, Prabhakar Venkatraman
9,899,089	Memory architecture having two independently controlled voltage pumps; Hirose Ryan Tasuo, Jenne Fredrick B., Raghavan Vijay, **Kouznetsov Igor G.**, Ruth Paul Fredrick, Zonte Cristinel, Georgescu Bogdan L., Gitlan Leonard Vasile, Myers James Paul
9,847,137	Method to reduce program disturbs in non-volatile memory cells; Hirose Ryan T., **Kouznetsov Igor G.**, Prabhakar Venkatraman, Shakeri Kaveh, Georgescu Bogdan
9,818,484	Systems, methods, and apparatus for memory cells with common source lines; Yu Xiaojun, Prabhakar Venkatraman, **Kouznetsov Igor G**., Hinh Long T, Jin Bo
9,704,585	High voltage architecture for non-volatile memory; Georgescu Bogdan I., Moscaluk Gary P., Raghavan Vijay, **Kouznetsov Igor G.**
9,627,073	Systems, methods, and apparatus for memory cells with common source lines; Yu Xiaojun, Prabhakar Venkatraman, **Kouznetsov Igor G**., Hinh Long T, Jin Bo
9,620,516	Embedded SONOS based memory cells; Ramkumar Krishnaswamy, **Kouznetsov Igor G.**, Prabhakar Venkatraman
9,466,374	Systems, methods, and apparatus for memory cells with common source lines; Yu Xiaojun, Prabhakar Venkatraman, **Kouznetsov Igor G**., Hinh Long T, Jin Bo
9,431,124	Method to reduce program disturbs in non-volatile memory cells; Hirose Ryan T., **Kouznetsov Igor G.**, Prabhakar Venkatraman, Shakeri Kaveh, Georgescu Bogdan

9,361,994 Method of increasing read current window in non-volatile memory; **Kouznetsov Igor**

9,356,035 Embedded SONOS based memory cells; Ramkumar Krishnaswamy, **Kouznetsov Igor G.**, Prabhakar Venkatraman

9,355,725 Non-volatile memory and method of operating the same; Jin Bo, Ramkumar Krishnaswamy, Yu Xiaojun, **Kouznetsov Igor**, Prabhakar Venkatraman

9,171,857 Dense arrays and charge storage devices; Lee Thomas H., Subramanian Vivek, Cleeves James M., **Kouznetsov Igor G**., Johnson Mark G., Farmwald Paul Michael

9,123,642 Method of forming drain extended MOS transistors for high voltage circuits; Lee Sungwon, **Kouznetsov Igor**, Kim Gyu-Chul

8,988,938 Method to reduce program disturbs in non-volatile memory cells; Hirose Ryan T., **Kouznetsov Igor G.**, Prabhakar Venkatraman, Shakeri Kaveh, Georgescu Bogdan I.

8,953,380 Systems, methods, and apparatus for memory cells with common source lines; Yu Xiaojun, Prabhakar Venkatraman, **Kouznetsov Igor**, Hinh Long, Jin Bo

8,853,765 Dense arrays and charge storage devices; Lee Thomas H., Subramanian Vivek, Cleeves James M., **Kouznetsov Igor G**., Johnson Mark G., Farmwald Paul Michael

8,796,098 Embedded SONOS based memory cells; Ramkumar Krishnaswamy, **Kouznetsov Igor G.**, Prabhakar Venkatraman

8,675,405 Method to reduce program disturbs in non-volatile memory cells; Georgescu Bogdan, Hirose Ryan T., **Kouznetsov Igor G**., Prabhakar Venkatraman, Shakeri Kaveh

8,542,541 Memory architecture having two independently controlled voltage pumps; Hirose Ryan T., Jenne Fredrick, Srinivasaraghavan Vijay, **Kouznetsov Igor G.**, Ruths Paul Fredrick, Zonte Cristinel, Georgescu Bogdan, Gitlan Leonard Vasile, Myers James Paul

8,125,835 Memory architecture having two independently controlled voltage pumps; Hirose Ryan T., Jenne Fredrick, Raghavan Vijay, **Kouznetsov Igor G.**, Ruths Paul Fredrick, Zonte Cristinel, Georgescu Bogdan I., Gitlan Leonard Vasile, Myers James Paul

8,093,128 Integration of non-volatile charge trap memory devices and logic CMOS devices; Koutny Jr. William W.C., Geha Sam, **Kouznetsov Igor**, Ramkumar Krishnaswamy, Jenne Fredrick B., Levy Sagy, Karpe Ravindra, Warren Jeremy

7,969,804 Memory architecture having a reference current generator that provides two reference currents; Hirose Ryan T., Jenne Fredrick, Srinivasaraghavan Vijay, **Kouznetsov Igor G.**, Ruths Paul Fredrick, Zonte Cristinel, Georgescu Bogdan, Gitlan Leonard Vasile, Myers James Paul

7,825,455 Three terminal nonvolatile memory device with vertical gated diode; Lee Thomas H., Subramanian Vivek, Cleeves James M., Johnson Mark G., Farmwald Paul M., **Kouznetsov Igor G.**

7,615,436 Two mask floating gate EEPROM and method of making; **Kouznetsov Igor G**., Walker Andrew J.

7,339,848 Anti-fuse latch circuit and method including self-test; Stansell Galen, Jenne Fredrick, **Kouznetsov Igor**, Fox Ken

6,897,514 Two mask floating gate EEPROM and method of making; **Kouznetsov Igor G**., Walker Andrew J.

6,888,750 Nonvolatile memory on SOI and compound semiconductor substrates and method of fabrication; Walker Andrew J., Johnson Mark G., Knall N. Johan, **Kouznetsov Igor G.**, Petti Christopher J.

6,704,235 Anti-fuse memory cell with asymmetric breakdown voltage; Knall N. Johan, Cleeves James M., **Kouznetsov Igor G.**, Vyvoda Michael A.

6,531,366 Method and structure for high-voltage device with self-aligned graded junctions; **Kouznetsov Igor**